In the Claims:

1. (canceled)

2. (currently amended) A process of initializing the state of ~~an output memory circuit~~ latchable output buffer of a scan cell located at the boundary of a logic circuit within an integrated circuit having a logic circuit comprising:

A. scanning data into an input memory circuit of the scan cell while maintaining the scan cell in a first mode ~~providing normal operation~~ that enables connection of the logic circuit to the latchable output buffer;

B. placing the scan cell in a second mode that disables ~~normal operation of~~ connection of the logic circuit to the latchable output buffer; ~~and~~

C. enabling transfer of ~~transferring~~ the data scanned into the input memory circuit into the ~~output memory circuit~~ latchable output buffer simultaneous with the placing the cell in a second mode ~~a mode that disables normal operation of the logic circuit~~; and

D. thereafter, disabling transfer of the data scanned into the input memory circuit into the latchable output buffer while maintaining the scan cell in the second mode.

3. (previously presented) The process of claim 2 in which the first mode is a preload scan operation and the second mode is a test operation.

4. (previously presented) The process of claim 2 in which the first memory circuit is a capture/shift memory circuit.

5. (cancelled)

6. (currently amended) The process of claim 2 in which the maintaining includes enabling a first transmission gate between the logic circuit and the ~~output memory circuit~~

latchable output buffer and disabling a second transmission gate between the input memory circuit and the ~~output memory circuit~~ latchable output buffer.

7. (currently amended) The process of claim 2 in which the placing includes disabling a first transmission gate between the logic circuit and the ~~output memory circuit~~ latchable output buffer and enabling a second transmission gate between the input memory circuit and the ~~output memory circuit~~ latchable output buffer.